PATENT APPLICATION

AMENDMENT UNDER 37 C.F.R. § 1.116
U.S. Application No. 09/653,070

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended) In an integrated circuit, ~~A~~an interconnect circuit for transmitting data signals; said interconnect circuit comprising:

a data line transmitting said data signals in ~~an~~ said integrated circuit; and

a congestion line transmitting congestion signals;

wherein said data line selectively interrupts and reestablishes transmission of said data signals at selected portions of said data line responsive to said congestion signals.

2. (Original) An interconnect circuit according to claim 1 wherein said data line transmits said data signals and said congestion line transmits said congestion signals in opposite directions.

3. (Original) An interconnect circuit according to claim 1 wherein said data line is adapted for temporarily storing said data signals during periods in which said transmission of said data signals is selectively interrupted.

4. (Original) An interconnect circuit according to claim 1 further comprising:

a first terminal inputting said data signals into said data line; and

a second terminal receiving said data signals from said data line;

wherein said congestion signals are indicative of the status of said second terminal.

5. (Original) An interconnect circuit according to claim 4 wherein said congestion line transmits a congestion signal indicating that said second terminal cannot receive data at a slower speed than said congestion line transmits a congestion signal indicating that said second terminal can receive data.

6. (Original) An interconnect circuit according to claim 1 further comprising:

one or more additional data lines transmitting additional data signals;

wherein said additional data lines selectively interrupt and reestablish transmission of said additional data signals at selected portions of said additional data lines responsive to said congestion signals.

7. (Original) An interconnect circuit according to claim 6 wherein said data line and said one or more additional data lines are arranged in parallel.

8. (Original) An interconnect circuit according to claim 1 wherein said data line comprises a plurality of data driving circuits which selectively interrupt and reestablish transmission of said data signals responsive to said congestion signals and wherein said plurality of data driving circuits store said data signals temporarily when said transmission of said data signals is interrupted.

9. (Original) An interconnect circuit according to claim 8 wherein said plurality of data driving circuits are capable of arithmetical or logical functions.

10. (Original) An interconnect circuit according to claim 8 wherein said data line further comprises:

a first data driving circuit which interrupts transmission of said data signals responsive to a first congestion signal level and reestablishes transmission of said data signals responsive to a second congestion signal level; and

a second data driving circuit which interrupts transmission of said data signals responsive to a third congestion signal level and reestablishes transmission of said data signals responsive to a fourth congestion signal level.

11. (Original) An interconnect circuit according to claim 10 wherein said data line further comprises:

a plurality of first data driving circuits which interrupt transmission of said data signals responsive to said first congestion signal level and reestablish transmission of said data signals responsive to said second congestion signal level; and

a plurality of second data driving circuits which interrupt transmission of said data signals responsive to said third congestion signal level and reestablish transmission of said data signals responsive to said fourth congestion signal level;

wherein each of said plurality of first data driving circuits and each of said plurality of second data driving circuits are arranged in alternating fashion.

12. (Original) An interconnect circuit according to claim 10 wherein said congestion line supplies said first congestion signal level to said first data driving circuit and said third congestion signal level to said second data driving circuit.

13. (Original) An interconnect circuit according to claim 10 wherein said congestion line supplies said second congestion signal level to said first data driving circuit and said fourth congestion signal level to said second data driving circuit.

14. (Original) An interconnect circuit according to claim 10 wherein said first congestion signal level is equal to said fourth congestion signal level and said second congestion signal level is equal to said third congestion signal level.

15. (Currently amended) In an integrated circuit, ~~A~~an interconnect circuit comprising:

a data line transmitting data signals from a first terminal to a second terminal in ~~an~~ said integrated circuit; said data line comprising a plurality of data driving circuits selectively interrupting and reestablishing transmission of said data signals responsive to congestion signals; and

a congestion line supplying said congestion signals to each of said plurality of data driving circuits.

16. (Original) An interconnect circuit according to claim 15 wherein said congestion line comprises a plurality of secondary driving circuits transmitting said congestion signals in said congestion line in a direction opposite the direction of said transmission of said data signals.

17. (Original) An interconnect circuit according to claim 15 wherein said congestion line supplies said congestion signals to each of said plurality of data driving circuits in sequence from said second terminal proceeding to said first terminal.

18. (Original) An interconnect circuit according to claim 15 wherein said congestion signals are indicative of the status of said second terminal and wherein:

said plurality of data driving circuits interrupt transmission of said data signals responsive to a first congestion signal indicating said second terminal is not receiving data; and

said plurality of data driving circuits reestablish transmission of said data signals responsive to a second congestion signal indicating said second terminal is receiving data.

19. (Original) An interconnect circuit according to claim 18 wherein said first congestion signal is transmitted through said congestion line at a slower speed than said second congestion signal.

20. (Original) An interconnect circuit according to claim 16 wherein the number of said secondary driving circuits is different from the number of said data driving circuits.

21. (Original) An interconnect circuit according to claim 15 further comprising:

a plurality of additional data lines transmitting additional data signals from said first terminal to said second terminal and selectively interrupting and reestablishing transmission of said additional data signals responsive to said congestion signals.

22. (Original) An interconnect circuit according to claim 21 wherein said data line and said plurality of additional data lines are arranged in parallel.

23. (Original) An interconnect circuit according to claim 15 wherein said data driving circuits are adapted to store said data signals temporarily during the period when said transmission of said data signals is interrupted.

24. (Original) An interconnect circuit according to claim 15 wherein said data driving circuits are capable of arithmetical or logical functions.

25. (Original) An interconnect circuit according to claim 15 wherein said congestion line supplies said congestion signals at a first congestion signal level and a second congestion

signal level; said data line interrupting transmission of said data signals responsive to said first congestion signal level and reestablishing transmission of said data signals responsive to said second congestion signal level.

26. (Currently amended) In an integrated circuit, a~~A~~ method of transmitting data signals through an interconnect; said method comprising:

providing a data line for transmitting said data signals from a first terminal to a second terminal in an integrated circuit through a plurality of data driving circuits;

providing a congestion line for transmitting congestion signals to each of said plurality of data driving circuits; and

selectively interrupting and reestablishing transmission of said data signals at said plurality of data driving circuits responsive to said congestion signals.

27. (Original) A method according to claim 26 wherein said providing a congestion line further comprises providing a plurality of secondary driving circuits for transmitting said congestion signals in a direction opposite the direction of said transmission of said data signals.

28. (Original) A method according to claim 26 wherein said providing a data line further comprises enabling said plurality of data driving circuits to store said data signals temporarily when said transmission of said data signals is interrupted.

29. (Original) A method according to claim 26 wherein said transmitting congestion signals further comprises:

transmitting a first congestion signal indicating said second terminal is not receiving data; and

alternatively, transmitting a second congestion signal indicating said second terminal is receiving data;

wherein said first congestion signal is transmitted at a slower speed than said second congestion signal.

30. (Original) A method according to claim 26 further comprising:

providing a plurality of additional data lines for transmitting additional data signals from said first terminal to said second terminal; and

selectively interrupting and reestablishing transmission of said additional data signals responsive to said congestion signals.

31. (Original) A method according to claim 30 further comprising arranging said data line and said plurality of additional data lines in parallel.

32. (Original) A method according to claim 26 wherein said providing a data line includes providing said plurality of data driving circuits with arithmetical or logical function capabilities.